A1 Cont'd.

a source contact region, etched into the P^- well, and formed of an N^+ doped well and a P^+ doped well, wherein the P^+ doped well interfaces the N^- epitaxial layer and the P^- well, and the N^+ doped well is spaced apart from and located above the P^+ doped well;

whereby the snap-back is reduced and the avalanche-breakdown current endurance is increased.

4. (New) A method of manufacturing a power MOSFET device, comprising the steps of:

forming an N^- epitaxial layer on an N^+ silicon substrate;

forming a gate layer above the N^- epitaxial layer;

implanting a P^- dopant to form a P^- well in the N^- epitaxial layer;

forming an N^+ source region above the P^- well;

etching the N^+ source region and implanting a P^+ dopant to form a P^+ well, wherein the P^+ well interfaces the N^- epitaxial layer and the P^- well, and the N^+ source region is spaced apart from and located above the P^+ well;

depositing a glass layer; and

performing a metalization of the source contact and forming a drain contact;

whereby the snap-back is reduced and the avalanche-breakdown current endurance is increased.

5. (New) The method as claimed in claim 4, wherein the formation of the gate layer comprises the steps of:

etching a field oxide and growing a gate oxide layer;

depositing a polysilicon layer on the gate oxide layer, performing photomasking and etching the polysilicon layer.